Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of processing data comprising the step of:

coupling:

(a) at least one ~~(conventional)~~ unit adapted for processing data in a sequential manner and ~~, e.g. a CPU, von-Neumann-Processor and/or microcontroller, the (conventional) unit for data processing~~ comprising an instruction pipeline; [[,]] and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and a configurable network; [[,]]

wherein:

the unit is operable independently of the array; and

the array is:

at least one of ~~e.g. a preferrably~~ coarse ~~grain and/or preferrably~~ grained and runtime reconfigurable; and ~~data processor, FPGA, DFP, DSP, XPP or chaemeleon-technology-like data processing fabric, wherein the array is~~

coupled into [[to]] the instruction pipeline.

2. (Currently Amended) A method ~~in particular~~ according to claim 1, ~~wherein~~ further comprising the step of:

transferring via at least one data path at least one of [[the]] an input ~~and/or~~ and an output between the at least one ~~(conventional)~~ unit ~~processing data in a sequential manner, e.g. a CPU, von-Neumann-Processor, microcontroller,~~ and [[an]] the array, ~~for processing data comprising a plurality of data processing cells, e.g. a runtime and/or reconfigurable data processor, DFP, DSP, XPP or chaemeleon-technology-like data processing fabric, wherein data is transferred via~~ the at least one data path being provided therebetween and comprising at least one FIFO so as to allow for at least one of a ~~less tight~~ coupling between and a ~~and/or~~ data processing within the at least one unit and the array ~~two units~~ that is not strictly synchronous.

3. (Currently Amended) A method according to ~~any of the previous claims~~ claim 2, wherein the transferring is performed by at least one of inserting data directly into and extracting data directly from a ~~is transferred via at least one~~ data path ~~that allows for transfer~~ of at least one of the at least one unit and the array ~~data between units not being transferred through a register~~.

4. (Currently Amended) A method according to ~~any of the previous claims~~ claim 3, further comprising the step of:

providing between the at least one unit and the array ~~wherein~~ a path adapted for transfer ~~the transferal~~ of at least one of status information ~~and/or~~ and event information ~~such as flags, overflow, carry and the like is provided between the (conventional) unit for data processing and the at least one array for processing data~~.

5. (Currently Amended) A device for processing data comprising:

at least one ~~(conventional)~~ unit adapted for processing data in a sequential manner and ~~, e.g. a CPU, von-Neumann-Processor and/or microcontroller, the (conventional) unit for data processing~~ comprising an instruction pipeline; [[,]] and [[,]]

an array adapted for processing data comprising a configurable network and a plurality of data processing cells that are configurable in their function; ~~, e.g. a runtime and/or reconfigurable data processor, DFP, DSP, XPP or chaemeleon-technology-like data processing fabric,~~

wherein:

the array is coupled into [[to]] the instruction pipeline; and

the unit is operable independently of the array.

6. (Currently Amended) The device according to ~~the previous~~ claim 5, wherein at least one of:

at least one data path is provided between the array and the unit, the at least one data path ~~conventional processor~~ comprising at least one FIFO that allows ~~so as to allow for~~ at least one of a ~~less tight~~ coupling between and a ~~and/or~~ data processing within the at least one unit and the array ~~two units~~ that is not strictly synchronous; and ~~and/or wherein~~

data is transferred by at least one of extracting data directly from and inserting data directly into a data path of at least one of the at least one unit and the array ~~at least one data path is provided that allows for transfer of data not being transferred through a register~~.

7. (Currently Amended) A method of processing data comprising the steps of: coupling:

(a) at least one ~~(conventional)~~ unit adapted for processing data in a sequential manner and ~~, e.g. a CPU, von-Neumann-processor, microcontroller, being preferrably adapted for data processing, to any of the previous methods and or according to a previously claimed devices the (conventional) unit for data processing preferably~~ comprising an instruction pipeline; and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and a configurable network; and ~~, e.g. a runtime and/or reconfigurable data processor, DFP, DSP, XPP or chaemeleon-technology-like data processing fabric, wherein~~

providing a path allowing for block data transfer ~~is provided~~ from the array and at least one of a [[the]] data cache and another ~~and/or other~~ data source ~~and the array~~.

8-11. (Canceled).

12. (New) A method according to claim 1, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller.

13. (New) A method according to claim 1, wherein the array includes at least one of a data processor, a Field Programmable Gate-Array (FPGA), a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric.

14. (New) A method according to claim 2, wherein the at least one data path between the at least one unit and the array includes at least one local memory connected to the at least one unit as a cache and connected to the array.

15. (New) A method according to claim 14, wherein the at least one local memory includes an internal RAM (IRAM).

16. (New) A method according to claim 1, wherein configuration information for the array is issued by the instruction pipeline of the at least one unit.

17. (New) A method according to claim 16, further comprising:

buffering the configuration information in at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not strictly synchronous.

18. (New) A method according to claim 1, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit.

19. (New) A method according to claim 18, wherein the array is operable synchronously to the unit.

20. (New) A method according to claim 4, wherein the at least one of the status information and the event information includes at least one of flags, an overflow, and a carry.

21. (New) A device according to claim 5, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller.

22. (New) A device according to claim 5, wherein the array includes at least one of (a) a runtime and reconfigurable data processor, (b) a Data Flow Processor (DFP), (c) a Digital Signal Processor (DSP), (d) an eXtreme Processing Platform (XPP), and (e) a chaemeleon-technology data processing fabric.

23. (New) A device according to claim 6, wherein the at least one data path includes at least one local memory connected to the unit as cache and connected to the array.

24. (New) A method according to claim 23, wherein the at least one local memory includes an internal RAM (IRAM).

25. (New) A device according to claim 5, wherein configuration information for the array is issued by the instruction pipeline.

26. (New) A device according to claim 25, wherein the configuration information is buffered in at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not strictly synchronous.

27. (New) A device according to claim 5, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit.

28. (New) A device according to claim 27, wherein the array operates synchronously to the unit.

29. (New) A method according to claim 7, wherein the at least one unit includes at least one of a CPU, a von-Neumann-processor, and a microcontroller.

30. (New) A method according to claim 7, wherein the array includes at least one of a runtime and reconfigurable data processor, a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaemeleon-technology data processing fabric.